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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,911	09/27/2001	Jared Zerbe	00-167-A (RA194.CIP1.US)	2801

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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,911	ZERBE ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2005*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-41* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *35-41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the a) a multi-PAM output driver having a plurality of current-control ports; and b) a current-calibration circuit coupled to each of the current-control ports, the current-calibration circuit including a first, second, and third reference-voltage nodes; and c) a method of calibrating a multi-PAM output driver adapted to cause an output signal to transition between a plurality of logic states, the method comprising: dividing a reference voltage into a plurality of multi-PAM reference voltages on respective multi-PAM reference-voltage nodes, and shifting the logic states to allow equalization signals to overdrive transitions between the logic states, wherein shifting the logic states includes shifting the multi-PAM reference voltages' by drawing an offset current from one of the multi-PAM reference-voltage nodes. must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

As indicated by MPEP 201.06 (c), "....The specification and drawings of a continuation or divisional application filed under 37 CFR 1.53(b) are not limited to a reproduction or "true copy" of the prior application, i.e., the applicant may revise the specification for clarity or contextual purposes vis- à-vis the specification originally filed in the prior application in the manner that an applicant may file a substitute specification, see 37 CFR 1.125, or amend the drawings of an application so long as it does not result in the introduction of new matter..", so the Applicant may amend the drawings to show features for clarity or contextual purposes. In this case the Applicant has to, since the drawings that show claimed features are not found in the instant application (same with the specification if necessary).

Specification

The modifications to the specification were received on 08/23/2005. These modifications are accepted by the Examiner.

Claim Rejections - 35 USC § 103

Due to the cancellation of claims 1-26 the rejection of the previous Office action are withdraw.

Claim Objections

Claims 36-38 are objected to because of the following informalities: in line 16 of claim 35 the recitation "ii." is improper; it is suggested to be changed to "iii.". Appropriate correction is required.

Claims 39-41 are objected to because of the following informalities: in line 1 of claim 39 the recitation "method of calibrating" is improper; it is suggested to be changed to "method for calibrating". Appropriate correction is required.

Allowable Subject Matter

Claims 27-41 are allowed over prior art (if the above objections are overcome).

The following is an examiner's statement of reasons for allowance: claims 27-41 are allowed because the references cited fail to teach, as applicant has, a multi-PAM output driver having a plurality of current-control ports, a current-calibration circuit coupled to each of the current-control ports, the current-calibration circuit including a first, second, and third reference-voltage nodes, and a multi-level voltage generator including a voltage divider having first, second, third, and fourth resistors coupled in series to divide a reference voltage into a first multi-PAM reference voltage between the first and second resistors and coupled to the first reference-voltage node, a second multi-PAM reference voltage between the second and third resistors and coupled to the second reference-voltage node, and a third multi-PAM reference voltage between the third and fourth resistors and coupled to the third reference-voltage node, and an active

current source having a current-handling terminal and a current-control terminal, wherein the current-handling terminal is coupled between two of the first, second, third, and fourth resistors; a current-calibration circuitry for a multi-PAM output driver comprising a current-calibration circuit including a first, second, and third reference-voltage nodes adapted to receive respective relatively high, medium, and low reference voltages, and a multi-level voltage generator adapted to produce the high, medium, and low reference voltages, the voltage generator including first and second voltage supply pins providing a reference voltage, a voltage divider having first, second, and third multi-PAM reference terminals, the voltage divider dividing the reference voltage into a plurality of multi-PAM references, including a first multi-PAM reference voltage on the first multi-PAM reference terminal, a second multi-PAM reference voltage on the second multi-PAM reference terminal, and a third multi-PAM reference voltage on the third multi-PAM reference terminal; and an active current source drawing current from the first multi-PAM reference terminal to reduce the first multi-PAM reference voltage; and a shifting logic states to allow equalization signals to overdrive transitions between the logic states including shifting a multi-PAM reference voltages by drawing an offset current from one of the multi-PAM reference-voltage nodes, as the applicant has claimed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Koazechi (US 5568045 A) discloses a reference voltage generator, which includes a pair of bipolar transistors, a resistor circuit coupled to the

bipolar transistors to make them operative in different current densities from each other to thereby produce a voltage relative to a difference in base-emitter voltage between the transistors, and an operational amplifier coupled to receive the voltage to control a current flowing through the resistor circuit, and further includes a level shifter inserted between the resistor circuit and the operational amplifier to receive and shift the voltage from the resistor circuit, the level shifter thereby shifting the voltage to produce a level-shifted voltage and the operational amplifier receiving the level-shifted voltage. Koazechi doesn't disclose a multi-PAM output driver having a plurality of current-control ports; and a current-calibration circuit coupled to each of the current-control ports, the current-calibration circuit including a first, second, and third reference-voltage nodes.

This application is in condition for allowance except for the following formal matters:

See above.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
09-15-2005

KEVIN BURD
PRIMARY EXAMINER